

IN THE CLAIMS

The following listing of Claims replaces all prior listings of Claims previously presented:

Claim 1. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a silicide layer having an NiSi phase on source and drain regions in a semiconductor substrate, where the junction depth of the source and drain regions is from 20 nm to 60 nm below the lower surface of the silicide layer; and

after the formation of the silicide layer having the NiSi phase, performing manufacturing steps at a temperature not exceeding a critical temperature T_c , which meets the following expression:

$$T_c = a \times D_j + b,$$

$$\text{where } a = 6.11 \text{ (} 20 < D_j \leq 26 \text{)}$$

$$= 1.60 \text{ (} 26 < D_j \leq 60 \text{)},$$

$$b = 290.74 \text{ (} 20 < D_j \leq 26 \text{)}$$

$$= 408 \text{ (} 26 < D_j \leq 60 \text{)},$$

D_j is a junction depth (nm) measured from the lower surface of the silicide layer, and

T_c is a critical temperature ($^{\circ}\text{C}$) during a heat treatment.

Claim 2 (Withdrawn) The method of manufacturing a semiconductor device according to claim 1, wherein after the formation of the silicide layer having the NiSi phase, a silicon nitride layer is deposited so as to cover the silicide layer.

Claim 3. (Withdrawn) The method of manufacturing a semiconductor device according to claim 2, wherein an insulating layer is formed on the silicon nitride layer, and the insulating layer and the silicon nitride layer are selectively etched and removed by an RIE method so as to form openings reaching the source and drain regions through the insulating layer and the silicon nitride layer.

Claim 4. (Withdrawn) The method of manufacturing a semiconductor device according to claim 1, wherein an insulating layer is formed on the silicide layer having the NiSi phase, an opening reaching the silicide layer having the NiSi phase is formed through the insulating layer, and the opening is filled with copper by a coating method, thereby forming an electrode.

Claim 5. (Withdrawn) The method of manufacturing a semiconductor device according to claim 4, wherein before copper is filled in the opening, an inside of the opening is subjected to a plasma containing NF_3 , and then a barrier metal layer is formed over an interior of the opening including a bottom portion thereof by a sputtering method without subjecting the inside of the opening to the atmosphere.

Claim 6. (Currently Amended) A semiconductor device comprising a semiconductor element including:

a gate electrode formed on a silicon semiconductor substrate;
source and drain regions formed at both sides of the gate electrode in the silicon semiconductor substrate; ~~and~~
an NiSi layer formed on the source and drain regions;[[,]]
an insulating layer formed on the NiSi layer; and

a plug of a metal material containing copper formed in the insulating layer so as to be electrically in contact with the NiSi layer,

~~where~~ wherein a junction depth of the source and drain regions ~~being~~ ranges from 20 nm to 60 nm from a lower surface of the NiSi layer, Ni atoms ~~existing~~ exist in the source and drain regions, and a concentration of the Ni atoms at the junction depth being at $1.6 \times 10^{14} \text{ cm}^{-3}$ or less.

Claim 7. (Original) The semiconductor device according to claim 6, wherein the concentration of the Ni atoms in the silicon semiconductor substrate at a portion 10 nm in depth from the lower surface of the NiSi layer is at $5 \times 10^{18} \text{ cm}^{-3}$ or more, and $3 \times 10^{21} \text{ cm}^{-3}$ or less.

Claim 8. (Original) The semiconductor device according to claim 6, further comprising a silicon nitride layer formed to cover the NiSi layer and to have an optical refractive index of 1.89 or less.

Claim 9. (Canceled)

Claim 10. (Original) The semiconductor device according to claim 6, wherein the gate electrode is completely formed of the NiSi layer.

Claim 11. (Original) The semiconductor device according to claim 6, wherein a plurality of the semiconductor elements are formed on the silicon semiconductor substrate, each being isolated by an insulating layer filling up shallow trenches formed in the silicon semiconductor substrate.

Claim 12. (Currently Amended) The semiconductor device according to claim 11, wherein n-type MOSFETs and p-type MOSFETs ~~constituting~~ constitute a logic circuit.

Claim 13. (Original) The semiconductor device according to claim 7, further comprising a silicon nitride layer formed to cover the NiSi layer and to have an optical refractive index of 1.89 or less.

Claim 14. (Canceled).

Claim 15. (Original) The semiconductor device according to claim 7, wherein the gate electrode is completely formed of the NiSi layer.

Claim 16. (Original) The semiconductor device according to claim 7, wherein a plurality of the semiconductor elements are formed on the silicon semiconductor substrate, each being isolated by an insulating layer filling up shallow trenches formed in the silicon semiconductor substrate.

Claim 17. (Currently Amended) The semiconductor device according to claim 16, wherein n-type MOSFETs and p-type MOSFETs ~~constituting~~ constitute a logic circuit.

Claim 18. (Currently Amended) The semiconductor device according to claim 6, further comprising an insulating layer, having a dielectric constant of 3.9 or more, between the gate electrode and the silicon semiconductor substrate.

Claim 19. (Currently Amended) The semiconductor device according to claim 7, further comprising an insulating layer, having a dielectric constant of 3.9 or more, between the gate electrode and the silicon semiconductor substrate.